	Application No.	Applicant(s)
Notice of Allowability		
	10/660,903 Examiner	LANGHAMMER, MARTIN Art Unit
	LAdiminer	Artome
	Chat C. Do	2193
The MAILING DATE of this communication apper All claims being allowable, PROSECUTION ON THE MERITS IS herewith (or previously mailed), a Notice of Allowance (PTOL-85) NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RI of the Office or upon petition by the applicant. See 37 CFR 1.313	(OR REMAINS) CLOSED in this or other appropriate communica GHTS. This application is subje	s application. If not included ation will be mailed in due course. THIS
1. This communication is responsive to <u>05/21/2007</u> .		
2. The allowed claim(s) is/are 1 and 3-4 now re-numbered as	<u>1-3</u> .	
3. Acknowledgment is made of a claim for foreign priority un	ider 35 U.S.C. § 119(a)-(d) or (f)	) <b>.</b>
a) ☐ All b) ☐ Some* c) ☐ None of the:		
1.   Certified copies of the priority documents have	been received.	
2. Certified copies of the priority documents have been received in Application No		
3. Copies of the certified copies of the priority documents have been received in this national stage application from the		
International Bureau (PCT Rule 17.2(a)).		
* Certified copies not received:		
Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.  THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.		
4. A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.		
5. CORRECTED DRAWINGS (as "replacement sheets") must be submitted.		
(a) ☐ including changes required by the Notice of Draftspers		TO-948) attached
1)  hereto or 2)  to Paper No./Mail Date		
(b) ☐ including changes required by the attached Examiner's Paper No./Mail Date		he Office action of
Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).		
6. DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.		
Attachment(s) 1. ☐ Notice of References Cited (PTO-892)	5  Notice of Inform	nal Patent Application
	6. ☑ Interview Sumn	• •
2. Notice of Draftperson's Patent Drawing Review (PTO-948)	Paper No./Mai	l Date <u>attached herein</u> .
<ol> <li>Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date</li> </ol>	7. 🛛 Examiner's Am	endment/Comment
Examiner's Comment Regarding Requirement for Deposit of Biological Material	8. 🛛 Examiner's Sta	tement of Reasons for Allowance
•	9. 🔲 Other	M
		Chat C. Do
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## **EXAMINER'S AMENDMENT**

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with James W. Rose Reg. No. 34,239 on 07/17/2007.

The application has been amended as follows:

1. (Currently Amended) A programmable logic device (PLD) including a plurality of logic array blocks (LAB's) connected by a PLD routing architecture, wherein at least one LAB is configured in different modes of operations to determine a compression of a plurality of N-bit numbers, the one LAB comprising:

a plurality of look-up table (LUT) logic cells, each look-up table (LUT) logic cell configured to input three operand signals at three respective inputs of that look-up table (LUT) logic cell and to output two signals at two respective outputs of that look-up table logic cell (LUT) that are a sum and carry signal resulting from adding the three operand input signals; input lines configured to receive input signals from the PLD routing architecture that represent the plurality of N-bit numbers and output lines configured to provide output signals to the PLD routing architecture that represent the compression of the plurality of N-bit numbers; and

LAB internal routing logic, not part of the routing architecture of the PLD, connecting the LUT logic cells such that the LUT logic cells collectively process the input signals, received at the input lines, that represent the N-bit numbers to generate the output signals, provided at the output lines, that represent the sum of the N-bit numbers; and

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<u>a register on the outputs and multiplexor and control bits internally to switch</u> between different modes of operations,

wherein the LUT logic cells are organized into slices, each of the slices
performing arithmetic on a bit position of the operand signals, each slice including two of
the plurality of LUT logic cells organized in a cascaded arrangement,

the first logic cell in each slice performing processing of three lines receiving a first one of the bits of the N-bit numbers, and

the second logic cell in each slice performing processing of three line receiving a second one of the bits of the N-bit numbers.

- 2. (Canceled)
- 2. Claims 2 and 5 are canceled.
- 3. Claims 1 and 3-4 are allowed.
- 4. The following is an examiner's statement of reasons for allowance:

The prior art of records fails to disclose or render an obviousness of a programmable logic device including a plurality of LAB for compressing N-bit numbers, each LAB comprising: a plurality of LUT logic cells configured to take three operand input signals and generate two output signals that corresponding to the sum and carry signal resulting from adding the three operand input signals; wherein the LUT logic cells are organized into slices, each of the slices performing arithmetic on a bit position of the operand signals, each slice including two of the plurality of LUT logic cells organized in a cascaded arrangement, the first logic cell in each slice performing processing of three lines receiving a first one of the bits of the N-bit numbers, and the second logic cell in each slice performing processing of three line receiving a second one of the bits of the N-bit numbers along with other features cited in the independent claim 1.

The closest found prior art is Pedersen (U.S. 6,066,960). Pedersen also discloses a PLD having a plurality of LAB for compressing N-bit numbers, however Pedersen fails to disclose the structure of each LAB as seen in above.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on Tue-Fri 9:00AM to 7:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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July 18, 2007

AAT.